Sub B1

1. ~~An interrupt request controller for processing a~~ plurality of interrupt logic signals, such controller, comprising:

a programmable bit masking section fed by the interrupt logic signals, adapted to mask selected ones of the interrupt signals;

a interrupt priority section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively ~~in~~ accordance with a predetermined priority criteria.

2. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals.

3. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith.

4. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt

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~~logic signals representative of whether the logic state of~~ the interrupt logic signal should remain as an edge or be converted to a level and for producing a corresponding output logic interrupt signal in accordance therewith.

5. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals;

a programmable bit masking section coupled to the programmable assertion sense/assertion type section, adapted to mask selected ones of the interrupt signals;

a interrupt priority section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined priority criteria.

6. The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals an interrupt sense register for storing a bit representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted.

7. The interrupt request controller recited in claim 6 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of whether the logic state of

~~the interrupt logic signal should remain as an edge or be converted to a level.~~